In the Claims

Claims

Claims 1-30 (Canceled).

31. (Currently amended) Integrated circuitry comprising:

a substrate;

a plurality of spaced conductive layers over the substrate and comprising upper surfaces;

a low-K material disposed over the substrate and between the spaced conductive layers, an entirety of the low-K material being elevationally below the upper surfaces of the spaced conductive layers; ~~and~~

a dielectric material having a first portion disposed over the low-K material elevationally below and between the upper surfaces of the spaced conductive layers, and the dielectric material having a second portion disposed over the upper surfaces of the spaced conductive layers; and

an etch-stop layer being formed between the low-K material and the dielectric material, an entirety of the etch-stop layer being elevationally below the upper surfaces of the spaced conductive layers.

32. (Previously presented) The circuitry of claim 31 wherein the low-K material comprises a first low-K material and wherein the dielectric material comprises a second low-K material different from the first low-K material.

33. (Previously presented) The circuitry of claim 31 wherein the dielectric material comprises a hydrogen silsesquioxane material.

34. (Previously presented) The circuitry of claim 31 wherein the low-K material comprises a carbon-comprising silicon oxide material.

35. (Previously presented) The circuitry of claim 31 wherein the low-K material comprises a first low-K material and wherein the dielectric material comprises a second low-K material having the same composition as the first low-K material.

36. (Previously presented) The circuitry of claim 31 further comprising a barrier layer disposed between the low-K material and the dielectric material.

37. (Currently amended) The circuitry of claim 31 further comprising two barrier layers disposed between the low-K material and the dielectric material, and wherein one of the two barrier layers comprises the etch-stop layer.

38. (Previously presented) The circuitry of claim 31 further comprising at least two barrier layers disposed between the spaced conductive layers.

39. (Previously presented) The circuitry of claim 31 further comprising a barrier layer disposed between the upper surfaces of the spaced conductive layers and the dielectric material.

40. (Currently amended) The circuitry of claim 31 further comprising a barrier layer having a first portion disposed between the upper surfaces of the spaced conductive layers and the dielectric material, and a second portion of the barrier layer disposed between the low-K material and the dielectric material.

Claims 41-50 (Canceled).

51. (New) The circuitry of claim 31 further comprising a barrier layer formed between the etch-stop layer and the dielectric material.

52. (New) The circuitry of claim 31 wherein the etch-stop layer comprises a barrier layer.

53. (New) The circuitry of claim 31 wherein the etch-stop layer extends between two of the plurality of the spaced conductive layers.

54. (New) The circuitry of claim 31 wherein the plurality of the spaced conductive layers comprises sidewalls extending from the substrate to the upper surfaces, and further comprising a barrier layer formed between the sidewalls and the low-K material.

55. (New) The circuitry of claim 31 wherein the plurality of the spaced conductive layers comprises sidewalls extending from the substrate to the upper surfaces, and further comprising a barrier layer formed between the sidewalls and the dielectric material.

56. (New) The circuitry of claim 31 wherein the plurality of the spaced conductive layers comprises sidewalls extending from the substrate to the upper surfaces, and further comprising a barrier layer formed between the sidewalls and the etch-stop layer.

57. (New) The circuitry of claim 31 wherein the plurality of the spaced conductive layers comprises sidewalls extending from the substrate to the upper surfaces, and further comprising at least two barrier layers formed between the sidewalls and the dielectric material.

58. (New) The circuitry of claim 31 further comprising a barrier layer formed between the etch-stop layer and the dielectric material, and wherein the etch-stop layer comprises the same material as the barrier layer.

59. (New) The circuitry of claim 31 wherein the etch-stop layer is formed between the low-K material and the first portion of the dielectric material.